AMENDMENTS

In the Specification

None.

In the Claims

Please replace the claims with the following clean version of the entire set of pending claims, in accordance with 37 C.F.R. §1.121(c)(1)(i). Cancel all previous versions of any pending claim.

A marked up version showing amendments to any claims being changed is provided in one or more accompanying pages separate from this amendment in accordance with 37 C.F.R. §1.121(c)(1)(ii). Any claim not accompanied by a marked up version has not been changed relative to the immediate prior version, except that marked up versions are not being supplied for any added claim or canceled claim.

SUB ET

65. (Amended) An integrated circuit comprising:

a monocrystalline silicon substrate;

a roughened platinum layer over the substrate, the roughened platinum layer having a continuous surface characterized by columnar pedestals that are at least about 300Å tall; and

an intervening layer between the platinum layer and the substrate, the intervening layer comprising at least one of IrO_2, RuO_2, RhO_2, or OsO_2.

66. (Amended) The circuit of Claim 65 wherein the columnar pedestals terminate in dome-shaped tops.

67. (Amended) The circuit of Claim 65 wherein the columnar pedestals terminate in hemispherical tops.

74. (Amended) A capacitor comprising:

a first capacitor electrode over a monocrystalline silicon substrate;

a second capacitor electrode;

a dielectric layer between the first and second capacitor electrodes;

wherein at least one of the first and second capacitor electrodes comprise roughened platinum, the roughened platinum having a continuous surface characterized by columnar pedestals having heights greater than or equal to about one-third of a total thickness of the roughened platinum.

Cancel Claim 76

77. (Amended) The integrated circuit of claim 65 wherein the roughened platinum layer has a thickness of at least about 400Å, and less than about 600Å.

Add new Claims 78-85

78. (New) An integrated circuit comprising:

a semiconductive substrate;

a conductive node location disposed within the semiconductive substrate;

a first layer disposed over the semiconductive substrate and in electrical contact with the conductive node, the first layer comprising at least one of iridium, rhodium, ruthenium, palladium, osmium, silver, alloy, IrO_2, RuO_2, RhO_2, or OsO_2; and

a platinum alloy layer disposed over the first layer, the platinum alloy layer characterized by a continuous, roughened outer surface, where the platinum alloy layer comprising platinum and at least one of rhodium, iridium, ruthenium, palladium, osmium or silver.

79. (New) The integrated circuit of Claim 78 where the roughened platinum alloy layer has a thickness of at least about 400Å, and less than about 600Å.

80. (New) The integrated circuit of Claim 78 where the roughened platinum alloy layer has a thickness of at least about 400Å, and less than about 1000Å.

81. (New) The integrated circuit of Claim 78 where the roughened platinum alloy layer has a thickness of about 400Å or less.

82. (New) The int grated circuit of Claim 78, where the rough ned platinum alloy layer comprises columnar pedestal structures having heights greater than or equal to about one-third of a total thickness of the roughened platinum alloy layer.

83. (New) The integrated circuit of Claim 82, the columnar pedestal structures having heights of at least 300Å.

84. (New) The circuit of Claim 82 wherein the columnar pedestals terminate in dome-shaped tops.

85. (New) The integrated circuit of Claim 65, where the roughened platinum layer comprises a platinum alloy comprising platinum and at least one of rhodium, ruthenium or palladium.